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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,452	06/27/2003	Tom Xiaohai He	AB-233U4	6610

23845 7590 10/28/2005

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EXAMINER	
KIM, PAUL D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,452	HE ET AL.	
	Examiner	Art Unit	
	Paul D. Kim	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *1-14 and 28-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20,24 and 27* is/are rejected.

7)☒ Claim(s) *21-23,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is a response to the restriction requirement filed on 9/2/05.

Response to the Restriction Requirement

1. Applicant's election of Group II, claims 15-27, in the reply filed on 9/2/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 1-14 and 28-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9/2/05.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: --A METHOD OFMAKING AN ELECTRONIC MODULE--.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 15, 19, 20 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Bates et al. (US PAT. 6,635,958).

Bates et al. teach a process of making an electronic module comprising steps of: creating a redistributed surface (24) on an integrated circuit (20), including creating a redistribution layer comprising at least a layer of conductive redistribution material above at least some portions of a top face of the integrated circuit (20), which redistribution layer is electrically connected to the integrated circuit and includes conductive traces (28), mounting pads (26), and interconnect pads (34) as shown in Figs. 1-3; using at least some of the traces to position at least some of the interconnect pads along at least one edge of the redistributed surface; creating a layer of insulation (30 such as a lower layer) above at least some portions of the redistribution layer; mounting at least one secondary component (36) to at least one mounting pad; securing the integrated circuit to a substrate (40), which substrate includes electrical traces (44), wherein at least one trace terminates along at least one edge of the substrate as shown in Fig. 3; and electrically connecting at least one interconnect pad along at least one edge of the redistributed surface and at least one trace along at least one edge of the substrate, thereby electrically connecting the substrate to the integrated circuit as shown in Fig. 3 (see also col. 4,line 21 to col. 5, line 54).

As per claim 19 the at least one secondary component is a coil (equivalent with a wire).

As per claim 20 a first layer of insulation (30 such as an upper layer) on at least some portions of the top face of the integrated circuit as shown in Fig. 3.

As per claim 24 at least a layer of shielding material layer (38) is formed above at least some portions of the integrated circuit as shown in Fig. 3.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore (US PAT. 6,889,087) in view of Lin (US PAT. 6,511,865).

Moore teaches a process of making an electronic module such as a microstimulator (as per claim 16) comprising steps of: creating a redistributed surface on an integrated circuit (301), including creating a redistribution layer comprising at least a layer of conductive redistribution material above at least some portions of a top face of the integrated circuit, which redistribution layer is electrically connected to the integrated circuit and includes conductive traces, mounting pads, and interconnect pads as shown in Fig. 3; using at least some of the traces to position at least some of the interconnect pads along at least one edge of the redistributed surface; mounting at least one

secondary component to at least one mounting pad (307); securing the integrated circuit to a substrate (305), which substrate includes electrical traces, wherein at least one trace terminates along at least one edge of the substrate; and electrically connecting at least one interconnect pad along at least one edge of the redistributed surface and at least one trace along at least one edge of the substrate, thereby electrically connecting the substrate to the integrated circuit as shown in Fig. 3 (see also col. 4,line 66 to col. 6,line 7).

However, Moore fails to teach a process of creating a layer of insulation above at least some portions of the redistribution layer. Lin teaches a process of making an electronic module including a process of providing an insulative adhesive layer between a chip and a circuit in order to provide mechanical attachment between the electronic components. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify a process of fabricating electronic module of Moore by providing an insulative adhesive layer between the electronic components as taught by Lin in order to provide mechanical attachment between the electronic components.

As per claim 17 Moore also teach a core (309) comprising two separate halves such that one core half is secured to the redistributed surface of the integrated circuit and one core half is secured to a portion of the substrate and a wire (201) is wound around the core halves to create a coil assembly as shown in Fig. 3.

As per claim 18 At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the

shape of the core halves as recited in the claimed invention because Applicant has not disclosed that the shape of the core halves as recited in the claimed invention provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with Moore because the shape of the core halves as recited in the claimed invention would perform equally well with Moore. Therefore, it would have been an obvious matter of design choice to modify the shape of the core halves of Moore to obtain the invention as specified in claim 18.

As per claim 19 the at least one secondary component is a coil (equivalent with a wire).

8. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moore in view of Lin, and further in view of Kohno et al. (US PAT. 6,358,762).

Moore, modified by Lin, teaches all of the limitations as set forth above except a post-processing on a wafer containing multiple integrated circuits. Kohno et al. teach a process of making an electronic module including a process of post-processing until the wafer is scribed into separate chips, which are sealed by resin (see also col. 1,lines 15-20). Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify a process of fabricating electronic module of Moore, modified by Lin, by a post-processing as taught by Kohno et al. in order to separate the chips formed on the wafer.

Allowable Subject Matter

9. Claims 21-23, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul D. Kim whose telephone number is 571-272-4565. The examiner can normally be reached on Monday-Friday between 7:00 AM to 3:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul D Kim
Examiner
Art Unit 3729